IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 11 and 12 in accordance with the following:

1. (ORIGINAL) Signal generating circuitry comprising:

a first clocked element connected for receiving a clock signal and a first synchronised signal which changes its logic state synchronously with respect to said clock signal, and switchable by said clock signal between a responsive state, in which the element is operable in response to said state change in said first synchronised signal to change a logic state of a second synchronised signal produced thereby, and a non-responsive state in which no state change in the second synchronised signal occurs; and

a second clocked element connected for receiving said clock signal and said second synchronised signal, and switchable by said clock signal between a responsive state, in which the element is operable in response to said state change in said second synchronised signal to change a logic state of a third synchronised signal produced thereby, and a non-responsive state in which no state change in the third synchronised signal occurs;

wherein, when said clock signal has a first logic state the first clocked element has said non-responsive state and said second clocked element has said responsive state, and when said clock signal has a second logic state the first clocked element has said responsive state and said second clocked element has said non-responsive state.

2. (ORIGINAL) Circuitry as claimed in claim 1, wherein the clock signal has alternate first and second clock edges and changes at each first clock edge from said second logic state to said first logic state and changes at each second clock edge from said first logic state to said second logic state, and a switching time of said first clocked element is less than an interval between each second clock edge and the following first clock edge, and a switching time of said second clocked element is less than an interval between each first clock edge and its following second clock edge.

3. (ORIGINAL) Circuitry as claimed in claim 1, wherein each of said first and second clocked elements is a transparent or half latch element.

4. (ORIGINAL) Circuitry as claimed in claim 1, wherein said state change in said first synchronising signal is permitted to occur between a first clock edge and its following second clock edge or between a second clock edge and its following first clock edge.

5. (ORIGINAL) Circuitry as claimed in claim 1, further comprising an input circuit connected for receiving said clock signal and an input signal that is permitted to change its logic state a synchronously with respect to said clock signal and operable, following the said state change in the input signal, to bring about the said state change in said first synchronised signal synchronously with respect to said clock signal.

6. (ORIGINAL) Circuitry as claimed in claim 5, wherein said first synchronised signal is produced by a further clocked element in said input circuit, and a switching time of said further clocked element is greater than that of each of said first and second clocked elements.

7. (ORIGINAL) Circuitry as claimed in claim 6, wherein the switching time of said further clocked element is permitted to be greater than one or each of the said intervals.

8. (ORIGINAL) Circuitry as claimed in claim 6, wherein said further clocked element is a master/slave or full latch element.

9. (ORIGINAL) Circuitry as claimed in claim 6, wherein said further clocked element has a reset input to which said input signal is applied, a data input to which a signal having a predetermined logic state is applied, and a data output at which said first synchronised signal is produced, whereby said state change in said first synchronised signal occurs after said further clocked element is released from a reset condition by said state change in said input signal.

10. (ORIGINAL) Circuitry as claimed in claim 1, further comprising a third clocked element connected for receiving said clock signal and said third synchronised signal, and switchable by said clock signal between a responsive state, in which the element is operable in response to said state change in said third synchronised signal to change a logic state of a fourth synchronised signal produced thereby and a non-responsive state in which no state change in the fourth synchronised signal occurs;

said third clocked element having said responsive state when said clock signal has said second logic state and having said non-responsive state when said clock signal has said first logic state.

11. (CURRENTLY AMENDED) Clock recovery circuitry, adapted to receive a stream of serial data and operable to perform a repeating series of N cycles, where $N \geq 2$, each said cycle having a rising edge and a falling edge, said clock recovery circuitry comprising:

N rising-edge latches, each connected for receiving ~~a~~ said stream of serial data and each triggered at ~~a~~ said rising edge of a different one of the N cycles of said repeating series to take a rising-edge sample of the data;

N falling-edge latches, each connected for receiving said ~~the data~~ stream of serial data and each triggered, at ~~a~~ said falling edge of a different one of the N cycles of said repeating series, to take a falling-edge sample of the data; and

a sample processing circuit which processes the rising-edge and falling edge samples to recover a clock signal from the data steam.

12. (CURRENTLY AMENDED) Circuitry as claimed in claim 11, having:

a controller which generates N first synchronised signals, each said first synchronised signal having an active state for an individually corresponding one of the N cycles of the said repeating series and having an inactive state in each non-corresponding cycle of the series; and

N processing circuits, each comprising:

an input for receiving a different one of said N first synchronised signals;

a first clocked element connected for receiving a clock signal and said one first synchronised signal, and switchable by said clock signal between a responsive state, in which the element is operable in response to said state change in said first synchronised signal to change a logic state of a second synchronised signal produced thereby, and a non-responsive

state in which no state change in the second synchronised signal occurs;

a second clock element connected for receiving said clock signal and said second synchronised signal, and swtichable by said clock signal between a responsive state, in which the element is operable in response to said state change in said second synchronised signal to change a logic state of a third synchronised signal produced thereby, and a non-responsive state in which no state change in the third synchronised signal occurs;

a third clocked element connected for receiving said clock signal and said third synchronised signal, and switchable by said clock signal between a responsive state, in which the element is operable in response to said state change in said third synchronised signal to change a logic state of a fourth synchronise signal produced thereby, and a non-responsive state in which no state change in the fourth synchronised signal occurs;

wherein, when said clock signal has a first logic state the first and third clocked elements have said non-responsive state and said second clocked element has said responsive state, and when said clock signal has a second logic state the first and third clocked elements have said responsive state and said second clocked element has said non-responsive state; and

each of said N processing circuits further comprising:

one of said rising-edge latches connected to be enabled by one of said third and fourth synchronised signals; and

one of said falling-edge latches connected to ~~the~~ be enabled by the other of said third and fourth synchronised signals.

13. (ORIGINAL) Circuitry as claimed in claim 12, wherein the said controller comprises a circulating control register having N storage elements, each for storing one bit of an N-bit control pattern that is transferred in circular manner through the register, one bit of the said control pattern having a first value and each other bit having a second value, and each storage element providing one of the said output signals, which output signal has said active state when the bit of the control pattern stored in the storage element has said first value and which has said inactive state when that stored bit has said second value.

14. (ORIGINAL) Circuitry as claimed in claim 13 wherein each said storage element comprises an edge-triggered latch element which produces the said output signal.

15. (ORIGINAL) Verification circuitry, for connection to a circulating control register to verify that a predetermined N-bit control pattern is circulating correctly through the register, the register having N storage elements, each for storing one bit of the control pattern, and one bit of the control pattern having a first value and each other bit having a second value, the verification circuitry comprising:

a first check circuit, connected operatively to a first set of two or more consecutive storage elements of the register, and producing a first check signal which has a first state when any of the storage elements of the first set has said first value and which has a second state when all of the storage elements of the first set have said second value;

a second check circuit, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, and producing a second check signal which has a first state when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and

a same state detection circuit connected to said first and second check circuits and producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

16. (ORIGINAL) Circuitry as claimed in claim 15, wherein said first value is a zero and said second value is a one, and each said check circuit performs and AND or NAND operation on the respective stored values of the storage elements of its set.

17. (ORIGINAL) Circuitry as claimed in claim 15, wherein the said first value is a one and said second value is a zero, and each said check circuit performs an OR or NOR operation on the respective stored values of the storage elements of its set.

18. (ORIGINAL) Circuitry as claimed in claim 15, wherein said same state detection circuit operates to produce said detection signal at a predetermined detection time following a circulation operation of the control register when the states of the first and second check signals have stabilized.

19. (ORIGINAL) Data synchronising circuitry, for receiving successively first items of data and for outputting successively second items of data derived from the received first items, one of said first items being received in each cycle of a first clock signal and one of said second items being output in each cycle of a second clock signal having a frequency N times that of the first clock signal, where N is an integer, which circuitry comprises:

a reset signal generator which causes a reset signal to be changed from an active state to an inactive state at a preselected point in a first-clock-signal cycle;

a counter connected for receiving said second clock signal and said reset signal and operable, following the change of said reset signal to said inactive state, to count pulses of said second clock signal and to produce transfer control signals at intervals of N cycles of said second clock signal; and

a data converter connected for receiving said transfer control signals and said second clock signal, and operable to accept respective first items in response to successive said transfer control signals and to derive said second items from the received first items and to output one of said second items per second-clock-signal cycle.

20. (ORIGINAL) Circuitry as claimed in claim 19, wherein said first items of data each have N bits and said second items of data each have a single bit.

21. (ORIGINAL) Circuitry as claimed in claim 19, wherein said data converter is a parallel-to-serial converter.

22. (ORIGINAL) Circuitry as claimed in claim 19, wherein:

said counter comprises a circulating control register having N storage elements, each for storing one bit of an N-bit control pattern that is transferred in circular manner through the register in successive second-clock-signal cycles, one bit of said control pattern having a first value and each other bit having a second value; and

one of said transfer control signals is produced each time the bit of the control pattern stored in a predetermined one of the storage elements has said first value.

23. (ORIGINAL) Circuitry as claimed in claim 19, wherein said reset signal generator is connected for receiving both said first and said second clock signals and is operable to detect a preselected change in logic state of said first clock signal and, in response to such detection, to bring about said change of said reset signal from said active state to said inactive state in synchronism with said second clock signal.

24. (ORIGINAL) Circuitry as claimed in claim 19, wherein said reset signal generator comprises:

a first synchronising circuit connected for receiving said first clock signal and an input signal that is permitted to change its logic state asynchronously with respect to said first clock signal, and operable, following the said state change in the input signal, to bring about a change in logic state of a detection signal; and

a second synchronising circuit connected for receiving said second clock signal and said detection signal and operable, following said state change in said detection signal, to bring about the said change of said reset signal from said active state to said inactive state in synchronism with said second clock signal.

25. (ORIGINAL) Circuitry as claimed in claim 24, wherein said first synchronising circuit comprises a clocked element having a clock input to which said first clock signal is applied, a reset input to which said input signal is applied, a data input to which a signal having a predetermined logic state is applied, and a data output from which said detection signal is derived, whereby said state change in said detection signal occurs after said clocked element of said first synchronising circuit is released from a reset condition by said state change in said input signal.

26. (ORIGINAL) Circuitry as claimed in claim 24, wherein said second synchronising circuit comprises a clocked element having a clock input to which said second clock signal is applied, a reset input to which said input signal is applied, a data input to which said detection signal is applied, and a data output from which said reset signal is derived, whereby said state change in said reset signal occurs after said clock element of said second synchronising circuit is released from a reset condition by said state change in said input signal and after said state change in said detection signal.

27. (ORIGINAL) Data recovery circuitry, for sampling a received serial data stream, comprising:

a clock recovery circuit connected for receiving a plurality of candidate clock signals having the same frequency but spaced apart one from the next in phase, and operable to select, as a recovered clock signal, one of said candidate clock signals that matches said received serial data stream in phase;

an offset clock circuit operable to select, as an offset clock signal, a further one of said candidate clock signals different from said candidate clock signal selected as said recovered clock signal; and

a data sampling circuit operable to sample said received data stream using said offset clock signal.

28. (ORIGINAL) Circuit as claimed in claim 27, wherein said offset clock circuit is operable to select, as said offset clock signal, one of said candidate clock signals that leads said recovered clock signal in phase.

29. (ORIGINAL) Circuitry as claimed in claim 27, wherein said offset clock circuit is connected for receiving an offset clock signal and is operable to select said further one of said candidate clock signals in dependence upon the received offset clock signal.

30. (ORIGINAL) Circuitry as claimed in claim 29, wherein said offset control signal is a user-adjustable control signal.

31. (ORIGINAL) Circuitry as claimed in claim 29, wherein said clock recovery circuit generates a first selection signal for designating the candidate clock signal selected as said recovered clock signal, and said offset clock circuit generates a second selection signal, for designating the said further candidate clock signal selected as said offset clock signal, based on said first selection signal and said offset control signal.

32. (ORIGINAL) Circuitry as claimed in claim 31, wherein one or each of said first and second selection signals is a Gray-coded signal.

33. (ORIGINAL) Circuitry as claimed in claim 31, wherein said offset clock circuit comprises a modulo-N adder which adds said offset control signal to said first selection signal to produce said second selection signal, where N is the number of candidate clock signals in the said plurality.

34. (ORIGINAL) Circuitry as claimed in claim 27, wherein a maximum absolute phase difference between any two of said candidate clock signals of said plurality is 180°.

35. (ORIGINAL) Circuitry as claimed in claim 27, wherein said candidate clock signals of said plurality are spaced substantially equally in phase one from the next.

36. (ORIGINAL) Circuitry as claimed in claim 35, wherein a last one of the candidate clock signals of said plurality differs in phase from a first one of said candidate clock signals of said plurality by substantially the same amount as the two candidate clock signals of each further pair of mutually-adjacent candidate clock signals of said plurality differ in phase from one another.

37. (ORIGINAL) Circuitry as claimed in claim 27, further comprising a multiphase clock signal generator including:

a delay line, connected for receiving a reference clock signal having a frequency equal or close to a data rate of said serial data stream and having a series of individual delay stages from which said candidate clock signals are derived; and

a delay adjustment circuit which controls a total delay imposed by the delay stages of said series to be substantially equal to a duration of one cycle of said reference clock signal.

38. (ORIGINAL) Circuitry as claimed in claim 37, wherein said delay adjustment circuit receives a first phase comparison signal applied to an input of a first one of the delay stages of said series, and a second phase comparison signal produced at an output of a last one of the delay stages of said series, and is operable to control the said total delay so that said first and second phase comparison signals are maintained at substantially the same frequency but with transitions in said second phase comparison signal being substantially aligned with corresponding transitions in said first phase comparison signal.

39. (ORIGINAL) Circuitry as claimed in claim 37, wherein the delay stages of said series are fewer in number than said candidate clock signals of said plurality, and said multiphase clock signal generator further includes a phase interpolator connected for receiving a plurality of basic phase signals produced by the delay stages of said series and operable to produce a plurality of interpolated phase signals having phases intermediate between the respective phases of the basic phase signals.

40. (ORIGINAL) Circuitry as claimed in claim 27, wherein said clock recovery circuit compares the respective phases of said received serial data stream and the candidate clock signal currently selected as said recovered clock signal, and selects a next candidate clock signal from amongst the candidate clock signals of said plurality based on the comparison results.

41. (ORIGINAL) Circuitry as claimed in claim 27, wherein said clock recovery circuit comprises a digital phase lock loop circuit.

42. (ORIGINAL) Clock recovery circuitry as claimed in claim 13, further comprising verification circuitry connected to said circulating control register of said controller for verifying that said control pattern is circulating correctly therethrough, the verification circuitry comprising:

a first check circuit, connected operatively to a first set of two or more consecutive storage elements of the register, and producing a first check signal which has a first state when any of the storage elements of the first set has said first value and which has a second state when all of the storage elements of the first set have said second value;

a second check circuit, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, and producing a second check signal which has a first state when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and

a same state detection circuit connected to said first and second check circuits and producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

43. (ORIGINAL) Data synchronising circuitry as claimed in claim 22, further comprising verification circuitry connected to said circulating control register of said counter for verifying that said control pattern is circulating correctly therethrough, the verification circuitry comprising:

a first check circuit, connected operatively to a first set of two or more consecutive storage elements of the register, and producing a first check signal which has a first state when any of the storage elements of the first set has said first value and which has a second state when all of the storage elements of the first set have said second value;

a second check circuit, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, and producing a second check signal which has a first state when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and

a same state detection circuit connected to said first and second check circuits and producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.

44. (ORIGINAL) Verification circuitry, for connection to a circulating control register to verify that a predetermined N-bit control pattern is circulating correctly through the register, the register having N storage elements, each for storing one bit of the control pattern, and one bit of the control pattern having a first value and each other bit having a second value, the verification circuitry comprising:

first check means, connected operatively to a first set of two or more consecutive storage elements of the register, for producing a first check signal which has a first state when any of the storage elements of the first set has said first value and which has a second state when all of the storage elements of the first set have said second value;

second check means, connected operatively to the remaining storage elements of the register which form a second set of two or more consecutive storage elements, for producing a second check signal which has a first stage when any of the storage elements of the second set has said first value and which has a second state when all of the storage elements of the second set have said second value; and

same state detection means connected to said first and second check means for producing a detection signal, indicating that said control pattern is incorrect, when said first and second check signals have the same state.